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REMARKS

Claims 1-28 are all the claims pending in the application. Claims 8-28 are allowed. Claims 2-6 stand objected to only as being dependent upon a rejected base claim, and would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Claims 5 and 6 have been rewritten in independent form to place them in condition for immediate allowance. In addition, some of the limitations from allowable claim 2 have been incorporated into independent claim 1.

Claims 1 and 7 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejection

Claims 1 and 7 stand rejected under 35 U.S.C. §102(e) as being anticipated by Fried et al. (2003/0193058). Applicants respectfully traverse this rejection because Fried does not teach or suggest that the "first spacers are larger than said second spacers" or that "the difference in size between said first spacers and said second spacers is adapted to provide a difference between said first fin structure and said second fin structure", as defined by independent claim 1.

In Fried, the spacers 210 are the same size on each of the fins 206. As shown in Figures 5A-5B, insulator layers 210 are formed in a thermal oxidation process. Therefore, each of the insulator layers 210 will be the same size. For example, paragraph 50 of Fried explains that the insulator layers 210 are formed on opposing vertical sidewalls of the narrow and/or broad fins (i.e., semiconductor layer 206 portions) as depicted in FIGS. 5a-5b. Insulator layers 210 may be formed by thermal oxidation, typically at 750-800 °C., or alternatively, may be formed by depositing a dielectric film. Fried explains that, for the exemplary purposes of its disclosure, insulator layers 210 may be SiO₂, a nitrided oxide material, a high-K dielectric material, or combinations thereof, as known in the art. The insulator layers 210 on a narrow fin forms what may be the capacitive dielectric for a nominal-voltage decoupling capacitor.

Applicants respectfully submit that Fried does not teach or suggest that the "first spacers

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are larger than said second spacers" or that "the difference in size between said first spacers and said second spacers is adapted to provide a difference between said first fin structure and said second fin structure", as defined by independent claim 1. Therefore, independent claim 1 is patentable over Fried.

The claimed invention involves putting a spacer on the lower portion of some FinFETs (using a blocking mask to remove/reduce unwanted spacers), and by using several potential doping schemes, making the area protected behind the spacer electrically inactive. When a gate is subsequently patterned on top of the fin with spacers, a different width device is created than a fin without spacers. There is no limitation as to how many different height spacers could be placed on the wafer simultaneously, however there is an optimal number for balancing the design flexibility with the manufacturing costs.

The claimed process/structure produces a fin-type field effect transistor (FinFET) that has a buried oxide layer over a substrate, at least one first fin structure and at least one second fin structure positioned on the buried oxide layer. First insulating spacers are adjacent the first fin structures and second insulating spacers are adjacent the second fin structures. The first insulating spacers cover a larger portion of the first fin structure when compared to the portion of the second fin structure covered by the second insulating spacers.

Those fins that have larger spacers will receive a smaller area of active doping and those fins that have smaller spacers will receive a larger area of active doping. Therefore, there is a difference in doping between the first fins and the second fins that is caused by the differently sized spacers. The difference in doping between the first fins and the second fins changes an effective width of the second fins when compared to the first fins without having to use the fins of different physical widths or use multiple fins within each transistor, as is required conventionally.

These features are defined by independent claim one, which defines that the "first spacers are larger than said second spacers" or that "the difference in size between said first spacers and said second spacers is adapted to provide a difference between said first fin structure and said second fin structure." As explained above, it is Applicant's position that Fried does not teach or suggest these features. Therefore, Applicants respectfully submit that independent claim 1 is

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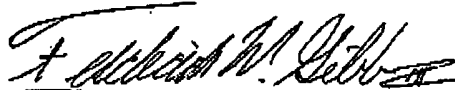
patentable over Fried and that dependent claim 7 is similarly patentable, not only because it depends from independent claim 1, but also because of the additional features of the invention it defines. In view of the foregoing, the examiner is respectfully requested to reconsider and withdraw this rejection.

In view of the foregoing, Applicants submit that claims 1-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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